OVERVIEW

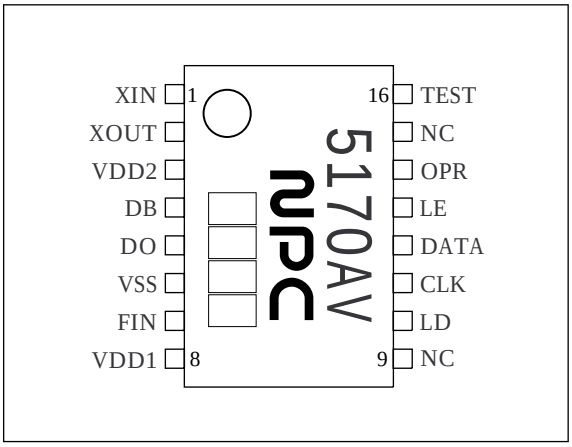
The SM5170AV is a PLL synthesizer IC developed for application in pagers. It incorporates independently-controlled reference frequency and FIN input frequency dividers, and operates from a low-voltage supply to realize low power dissipation. It features a charge pump that operates at 3 V, making possible a wide range of VCO designs.

FEATURES

- Supply voltages
  - V_{DD1} = 0.95 to 1.2 V (prescaler, counters)
  - V_{DD2} = 2.0 to 3.3 V (charge pump)
- FIN input frequency
  - f_{FIN} = 300 MHz (V_{DD1} = 0.95 V)
  - f_{FIN} = 330 MHz (V_{DD1} = 1.0 V)
- Reference frequency
  - f_{XIN} = 25 MHz (V_{DD1} = 0.95 V)
- 20 to 262140 reference frequency divider ratio range (with 1/4 prescaler built-in)
- 1056 to 131071 FIN input frequency divider ratio range
- –10 to 60 °C operating temperature range
- 16-pin VSOP

PINOUT

(Top view)



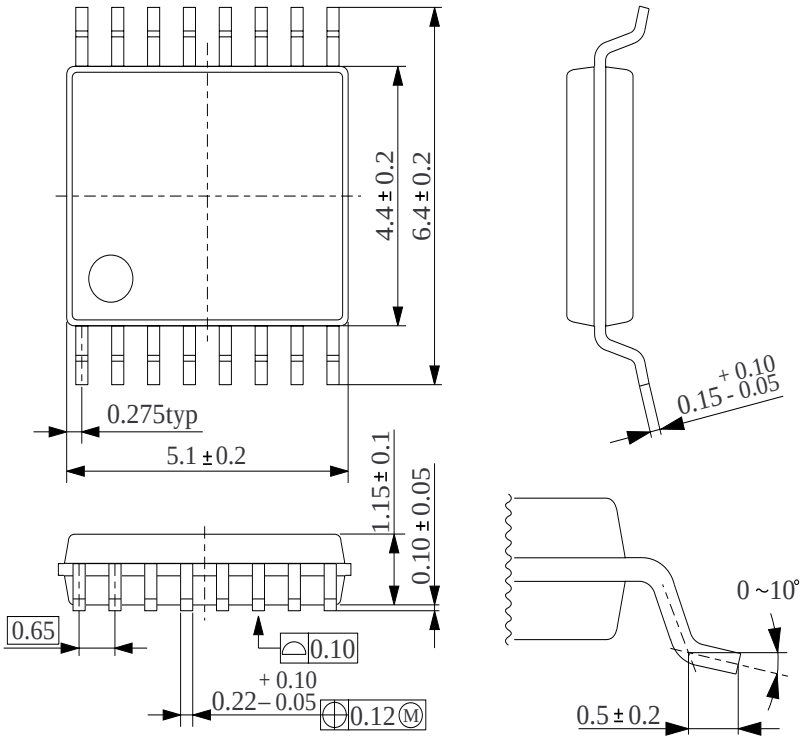
ORDERING INFORMATION

Device	Package
SM5170AV	16-pin VSOP

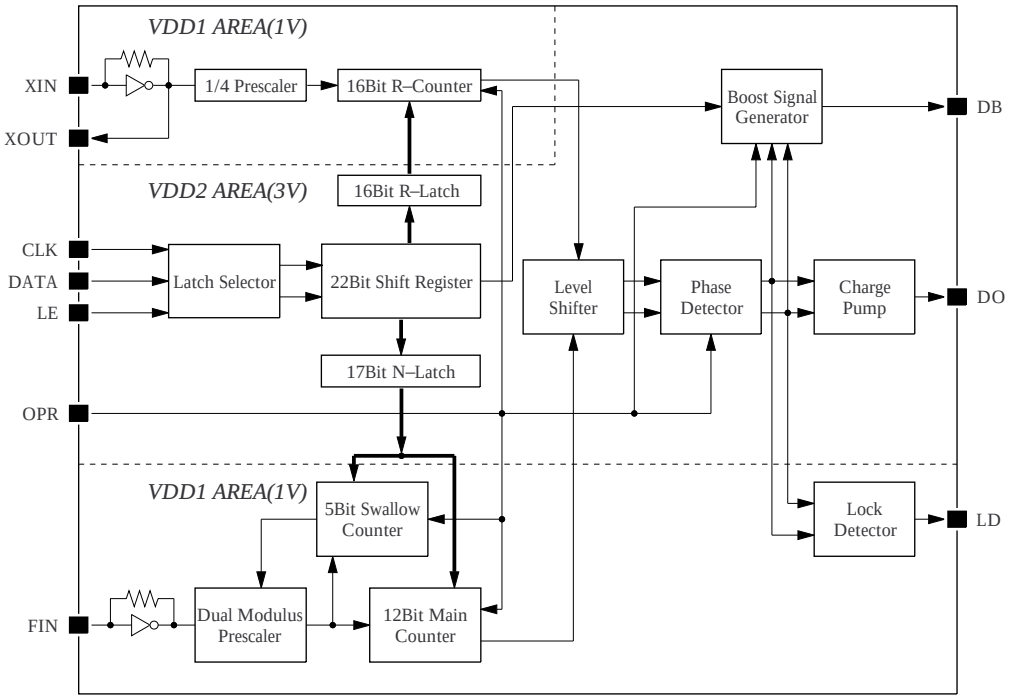
PACKAGE DIMENSIONS

Unit: mm

16-pin VSOP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Supply	Description
1	XIN	I	1 V	Reference frequency divider crystal oscillator connection pins. Alternatively, an external clock input can be connected to XIN. The clock is output on XOUT. Feedback resistor built-in for AC-coupled inputs.
2	XOUT	O	1 V	
3	VDD2	–	3 V	Phase comparator, charge pump and booster signal 3 V supply
4	DB	O	3 V	Booster signal output for faster locking
5	DO	O	3 V	Phase comparator output pin. Built-in charge pump and tristate output means that this output can be connected to a low-pass filter. The output polarity is preset for connection to a passive filter.
6	VSS	–	–	Ground pin
7	FIN	I	1 V	FIN input frequency divider input pin. Feedback resistor built-in for AC-coupled inputs.
8	VDD1	–	1 V	Reference frequency and FIN input frequency prescaler and counter 1 V supply
9	NC	–	–	No connection
10	LD	O	1 V	Unlock signal output pin. (Unlocked when LOW). The function of LD can be turned OFF using the LD input control bit (LD should be tied LOW when not used).
11	CLK	I	3 V	Control data clock input pin
12	DATA	I	3 V	Control data input pin
13	LE	I	3 V	Control data latch enable signal input pin
14	OPR	I	3 V	Power-save control pin. Start when HIGH, standby mode when LOW.
15	NC	–	–	No connection
16	TEST	I	1 V	Test pin. Pull-down resistor built-in. Leave open or connect to ground for normal operation.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD1}	VDD1	–0.3 to 2.0	V
	V_{DD2}	VDD2	–0.3 to 4.6	V
Input voltage range	V_{IN1}	FIN, XIN, TEST	V_{SS} – 0.3 to V_{DD1} + 0.3	V
	V_{IN2}	OPR, CLK, DATA, LE	V_{SS} – 0.3 to V_{DD2} + 0.3	V
Storage temperature range	T_{stg}		–40 to 125	°C
Power dissipation	P_D		150	mW

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD1}	VDD1	0.95 to 1.2	V
	V_{DD2}	VDD2	2.0 to 3.3	V
Operating temperature range	T_{opr}		–10 to 60	°C

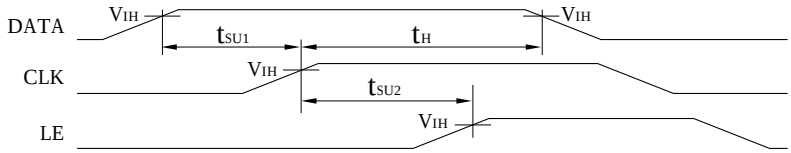
Electrical Characteristics

V_{SS} = 0 V, V_{DD1} = 0.95 to 1.2 V, V_{DD2} = 2.0 to 3.3 V, T_a = –10 to 60 °C

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
VDD1 operating current consumption	I_{DD1}	Note 1.		–	1.1	1.9	mA
VDD2 operating current consumption	I_{DD2}	Note 2.		–	0.003	–	mA
VDD1 standby current	I_{st1}	Note 3.		–	0.7	–	µA
VDD2 standby current	I_{st2}	Note 4.		–	0.01	10.0	µA
FIN maximum operating input frequency	f_{max1}	300 mVp-p sine wave	V_{DD1} = 0.95 to 1.2 V	300	–	–	MHz
			V_{DD1} = 1.0 to 1.2 V	330	–	–	MHz
XIN maximum operating input frequency	f_{max2}	300 mVp-p sine wave (external input)		25	–	–	MHz
FIN minimum operating input frequency	f_{min1}	300 mVp-p sine wave		–	–	40	MHz
XIN minimum operating input frequency	f_{min2}	300 mVp-p sine wave (external input)		–	–	9	MHz
FIN input amplitude	V_{FIN1}	f_{FIN} = 300 MHz, AC coupling		0.3	–	–	Vp-p
	V_{FIN2}	f_{FIN} = 330 MHz, V_{DD1} = 1.0 to 1.2 V, AC coupling		0.3	–	–	Vp-p
XIN input amplitude	V_{XIN}	f_{XIN} = 25 MHz, AC coupling (external input)		0.3	–	–	Vp-p
OPR, CLK, DATA, LE LOW-level input voltage	V_{IL}			–	–	0.3	V
OPR, CLK, DATA, LE HIGH-level input voltage	V_{IH}			V_{DD2} – 0.3	–	–	V
FIN LOW-level input current	I_{IL1}	V_{IL} = 0 V		–	–	60	µA
XIN LOW-level input current	I_{IL2}			–	–	10	µA
FIN HIGH-level input current	I_{IH1}	V_{IH} = V_{DD1}		–	–	60	µA
XIN HIGH-level input current	I_{IH2}			–	–	10	µA
DB LOW-level output voltage	V_{DOL}	Note 5.				0.5	V
DB HIGH-level output voltage	V_{DOH}	Note 6.		V_{DD2} – 0.5			V
DO LOW-level output current	I_{DOL}	Note 7.		1.0	–	–	mA
DO HIGH-level output current	I_{DOH}	Note 8.		1.0	–	–	mA
DO, DB tristate output high-impedance leakage current	I_{OZL}	V_{OL} = 0 V		–	–	100	nA
	I_{OZH}	V_{OH} = V_{DD2}		–	–	100	nA
DATA → CLK setup time	t_{SU1}	See the timing diagrams.		2	–	–	µs
CLK → LE setup time	t_{SU2}			2	–	–	µs
Hold time	t_H			2	–	–	µs

1. V_{DD1} = 1.0 to 1.05V, V_{DD2} = 2.7 to 3.3 V, f_{FIN} = 310 MHz (300 mVp-p sine wave), f_{XIN} = 14.4 MHz (300 mVp-p sine wave), 25 kHz comparator frequency, OPR = HIGH, no output load, typ condition : V_{DD1} = 1.0 V
2. V_{DD1} = 0.95 to 1.2 V, V_{DD2} = 2.7 to 3.3 V, f_{FIN} = 310 MHz (300 mVp-p sine wave), f_{XIN} = 14.4 MHz (300 mVp-p sine wave), 25 kHz comparator frequency, OPR = HIGH, no output load, typ condition : V_{DD2} = 3.0 V
3. V_{DD1} = 1.0 V, V_{DD2} = 3.0 V, OPR = LOW, no input/output load (i.e. CLK = DATA = LE = 0 V)
4. V_{DD1} = 0 V, V_{DD2} = 2.7 to 3.3 V, OPR = LOW, no input/output load (i.e. CLK = DATA = LE = 0 V), typ condition : V_{DD2} = 3.0 V
5. DB output is derived from the V_{DD2} supply. DB-pin condition select bit = $(00001)_2$, V_{DD2} = 2.7 to 3.3 V, no load
6. DB output is derived from the V_{DD2} supply. DB-pin condition select bit = $(11111)_2$, V_{DD2} = 2.7 to 3.3 V, no load
7. DO output is derived from the V_{DD2} supply. V_{DD2} = 2.7 to 3.3 V, V_{OL} = 0.4 V
8. DO output is derived from the V_{DD2} supply. V_{DD2} = 2.7 to 3.3 V, V_{OH} = V_{DD2} – 0.4 V

DATA, CLK, and LE timing



FUNCTIONAL DESCRIPTION

Frequency Divider Data

The input data should be specified keeping in mind the V_{DD2} supply. The data is input using CLK, DATA and LE pins into the shift register and latch which operate from the V_{DD2} supply. The V_{DD1} supply level, however, is not needed and can be ON or OFF.

The control data input uses a 3-line 24-bit serial interface comprising the clock (CLK), data input (DATA) and latch enable (LE). The data is input with the MSB first. The last two bits (23rd + 24th) are used as the latch select control bits. Data is written to the shift register on the rising edge of the clock signal. Accordingly, the data should change state on the falling edge of the clock signal. Data is transferred from the shift register to the latch when the latch enable (LE) signal goes HIGH. Accordingly, the latch enable signal should be held LOW while data is being written to the shift register.

The clock and data input signals are both ignored when the latch enable signal goes HIGH. Also, the CLK, DATA and LE inputs should be tied LOW when not setting data.

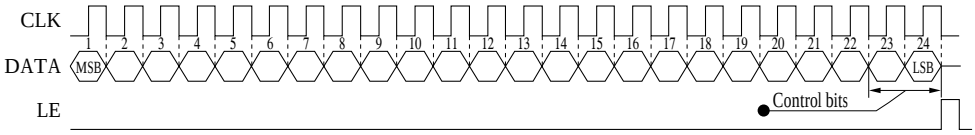


Figure 1. Frequency divider data format

Input Data Description

Latch select

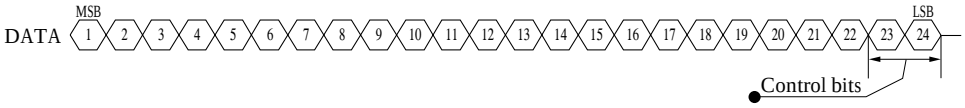


Figure 2. Latch select data format

The last two data bits determine the status of the shift register data latch.

Bit 23	Bit 24	Latch
0	0	Swallow counter and main counter frequency divider ratio latch select
0	1	Reference frequency counter divider ratio data and LD output latch select

FIN input frequency Divider (N-counter) Structure

The FIN input frequency divider generates a comparator frequency signal (FV), which is input to the phase comparator, by dividing the VCO signal input on pin FIN.

The phase comparator is comprised of dual modulus prescalers, a 5-bit swallow counter and a 12-bit main counter.

Frequency settings	Prescaler	P and P + 1
	Swallow counter	S
	Main counter	M
	FIN input frequency divider ratio	$N = (P + 1) \times S + P \times (M - S)$ $= P \times M + S$ (where $M > S$)
Counter set ranges	Prescaler	P = 32, P + 1 = 33
	Swallow counter	S = 0 to 31
	Main counter	M = 32 to 4095
FIN input frequency divider ratio range		N = 1056 to 131071

Swallow counter and main counter data

The swallow counter and main counter which determine the FIN input frequency divider ratio are set by bits 1 to 12 and bits 13 to 17, respectively. The voltage signal output on pin DB is set by bits 18 to 22.

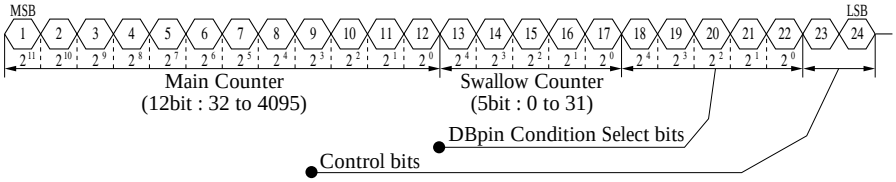


Figure 3. Swallow counter and main counter frequency divider data format

FIN input frequency divider example

If the VCO output is (f_{VCO}), the output frequency (f_{LO}) is 251.3 MHz, and the channel bandwidth (f_{CH}: Phase comparator frequency (f_R)) is 25 kHz, then the FIN input frequency divider ratio N is given by:

$$N = \frac{f_{LO}}{f_{CH}} = \frac{f_{VCO}}{f_N} = \frac{251.3}{0.025} = 10052$$
$$= 32 \times 314 + 4$$

Therefore, the swallow counter count is 4 $(00100)_2$ and the main frequency divider counter count is 314 $(000100111010)_2$.

DB fast-lockup data

The output voltage on pin DB provides an additional boost to charge the external lowpass filter capacitor for faster lockup times. One of 31 possible output voltage level signals is selected by bits 18 to 22.

The DB level signal output occurs during 2 clock cycles when the reference frequency divider comparator signal FR is generated after OPR goes HIGH, or after LE goes LOW when data is written. The DB output subsequently becomes high impedance.

Note that if bits 18 to 22 are all set to 0, this function is not activated and DB remains in the high impedance state.

Input data format example

FIN input frequency divider = 10052, DB is high impedance:

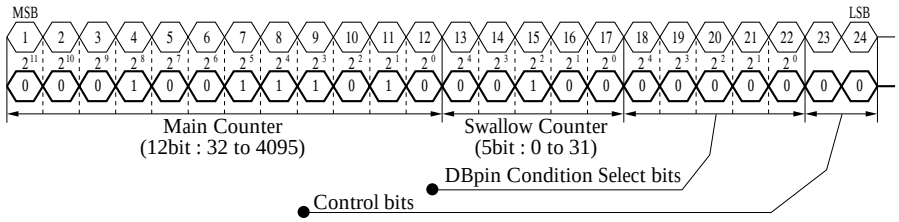


Figure 4. Swallow counter and main counter frequency divider data example

Reference Frequency Divider (R-counter) Structure

The reference frequency divider generates a comparator frequency signal (FR), which is input to the phase comparator, by dividing the reference oscillator frequency input either from an external signal on XIN or from a crystal oscillator connected between XIN and XOUT.

The reference frequency divider is comprised of a fixed divide-by-4 prescaler and a 16-bit reference counter.

Frequency settings	Prescaler	A (= 4)
	Reference counter	B
	Reference frequency divider ratio	$R = A \times B = 4 \times B$
Counter set ranges	Prescaler	A = 4
	Reference counter	B = 5 to 65535
Reference frequency divider ratio range		R = 20 to 262140

Reference counter frequency data and LD setting

The reference counter which determines the reference frequency divider ratio is set by bits 1 to 16. The lock detect signal output is set by bit 20.

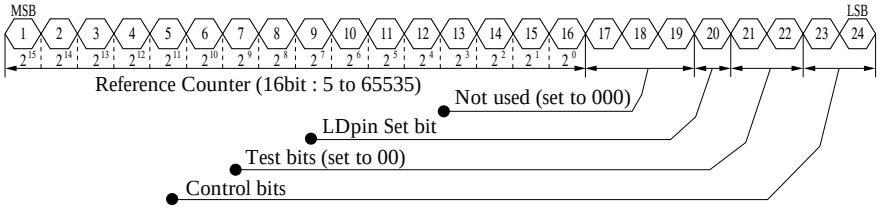


Figure 5. Reference counter data and LD output setting format

Reference frequency divider example

If the VCO output is (f_{VCO}), the crystal oscillator frequency is 14.4 MHz and the channel bandwidth (f_{CH}: comparator frequency (f_R)) is 25 kHz, then the reference frequency divider ratio R is given by:

$$R = \frac{Xtal}{f_{CH}} = \frac{Xtal}{f_R} = \frac{14.4}{0.025} = 576 = 4 \times 144$$

Therefore, the reference counter count is 144 $(0000000010010000)_2$.

LD output

The output on LD is set by bit 20.

Bit 20	LD output
1	Normal unlock signal output (normal operation)
0	Unlock signal output OFF, LOW-level output

Bits 15 to 19, bits 21 to 22

Bits 15 to 19 have no meaning, and should be set to 0. Bits 21 and 22 are factory test bits and should also be set to 0.

Input data format example

Reference frequency divider = 144, LD normal operation:

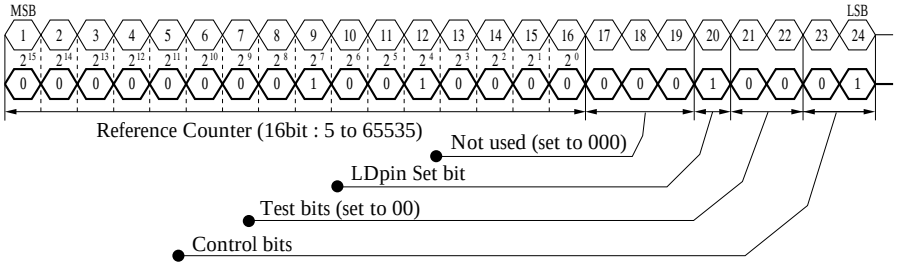


Figure 6. Reference counter data and LD output setting example

Standby Mode

The SM5170AV enters standby mode when OPR goes LOW. In this mode, the states and functions shown in the table occur.

Block	State
DO and DB	Floating (high impedance)
LD	LOW-level output
Phase comparator	Reset
Input FIN	Feedback resistor is cutoff (HIGH level)
Input XIN	Feedback resistor is cutoff (HIGH level)
N counter	Reset
R counter	Reset
Latch data	Stored (while V_{DD2} is within rating)

In standby mode, some current flows into VDD1. Therefore, it is necessary to reduce V_{DD1} to 0 V to fully reduce current consumption and reduce power dissipation. Note that if both the V_{DD1} and V_{DD2} supplies are reduced to 0 V, the latch contents will be erased. In this case, V_{DD1} only should be reduced to 0 V.

Standby mode is released when V_{DD1} rises and OPR goes HIGH.

Phase Comparator Timing Diagram

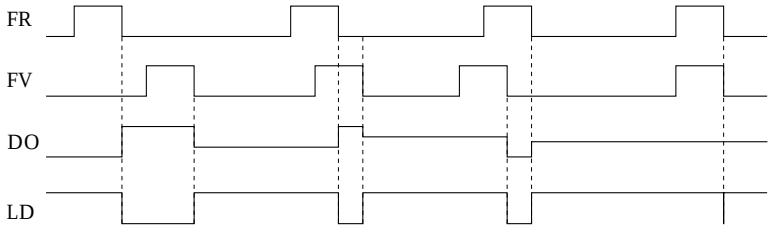
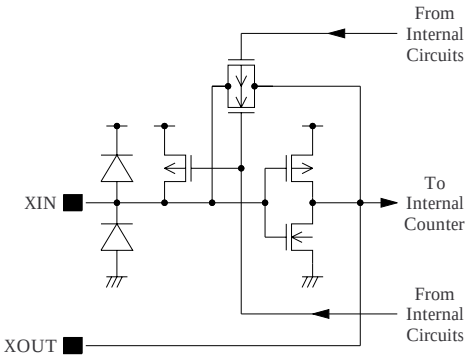


Figure 7. Phase comparator timing

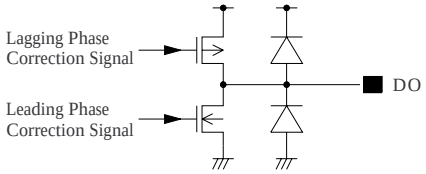
The DO output circuit polarity is configured for connection to an external passive filter.
The signals compared are FV and FR, which are the internal FIN input frequency divider output signal and reference frequency divider output signal, respectively.

INPUT/OUTPUT EQUIVALENT CIRCUITS

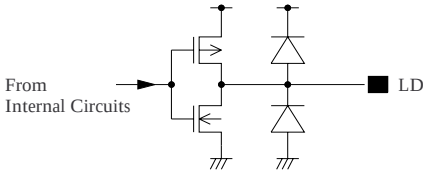
XIN, XOUT



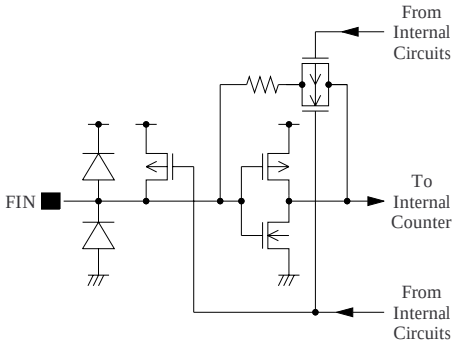
DO



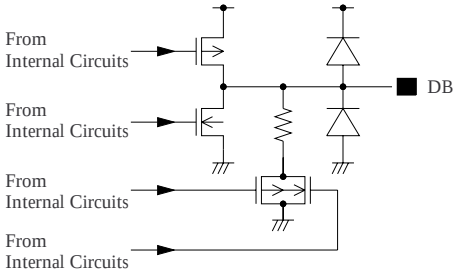
LD



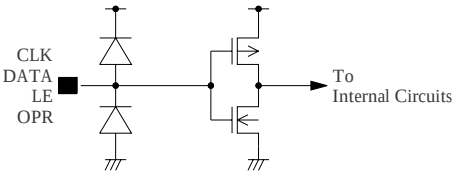
FIN



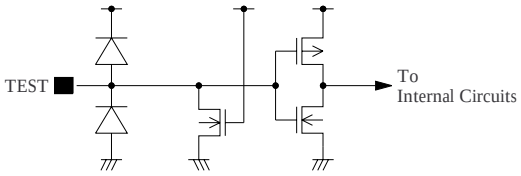
DB



OPR, CLK, DATA, LE



TEST



NIPPON PRECISION CIRCUITS INC. reserves the right to make changes to the products described in this data sheet in order to improve the design or performance and to supply the best possible products. Nippon Precision Circuits Inc. assumes no responsibility for the use of any circuits shown in this data sheet, conveys no license under any patent or other rights, and makes no claim that the circuits are free from patent infringement. Applications for any devices shown in this data sheet are for illustration only and Nippon Precision Circuits Inc. makes no claim or warranty that such applications will be suitable for the use specified without further testing or modification. The products described in this data sheet are not intended to use for the apparatus which influence human lives due to the failure or malfunction of the products. Customers are requested to comply with applicable laws and regulations in effect now and hereinafter, including compliance with export controls on the distribution or dissemination of the products. Customers shall not export, directly or indirectly, any products without first obtaining required licenses and approvals from appropriate government agencies.

NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

NC9808CE 1999.8